IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method for performing static timing analysis on an integrated circuit design, said method comprising:

performing static timing analysis on a final circuit netlist file utilizing a snip file, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis;

converting said snip file to a plurality of cutpoints after said final circuit netlist file met all timing constraints under said static timing analysis;

performing formal verification on said plurality of cutpoints;

determining whether or not said plurality of cutpoints pass said formal verification; ~~and~~

in response to a determination that said plurality of cutpoints do not pass said formal verification, issuing a flag to alert a user; and

in response to a determination that said plurality of cutpoints pass said formal verification, sending said final circuit netlist file to manufacturing.

2. (currently amended) The method of Claim 1, wherein said method further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, modifying said final circuit netlist file ~~list~~ and returning to said performing static timing analysis with said modified final circuit netlist file.

3. (original) The method of Claim 1, wherein said method further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, modifying said snip file and returning to said converting said snip file with said modified snip file.

Please cancel Claim 4.

5. (original) The method of Claim 1, wherein said performing formal verification further includes performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

Please cancel Claim 6.

7. (currently amended) A computer usable medium having a computer program product ~~residing on a computer usable medium~~ for performing static timing analysis on an integrated circuit design, said computer usable medium ~~program product~~ comprising:

program code means for performing static timing analysis on a final circuit netlist file utilizing a snip file, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis;

program code means for converting said snip file to a plurality of cutpoints after said final circuit netlist file met all timing constraints under said static timing analysis;

program code means for performing formal verification on said plurality of cutpoints;

program code means for determining whether or not said plurality of cutpoints pass said formal verification; ~~and~~

program code means for issuing a flag to alert a user, in response to a determination that said plurality of cutpoints do not pass said formal verification; and

program code means for sending said final circuit netlist file to manufacturing, in response to a determination that said plurality of cutpoints pass said formal verification.

8. (currently amended) The computer usable medium ~~program product~~ of Claim 7, wherein said computer program product further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, program code means for modifying said final circuit netlist file ~~list~~ and returning to said performing static timing analysis with said modified final circuit netlist file.

9. (currently amended) The computer usable medium ~~program product~~ of Claim 7, wherein said computer program product further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, program code means for modifying said snip file and returning to said converting said snip file with said modified snip file.

Please cancel Claim 10.

11. (currently amended) The computer usable medium ~~program product~~ of Claim 7, wherein said computer program product for performing formal verification further includes program code means for performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

Please cancel Claim 12.

13. (currently amended) A computer system for performing static timing analysis on an integrated circuit design, said computer system comprising:

means for performing static timing analysis on a final circuit netlist file utilizing a snip file, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis;

means for converting said snip file to a plurality of cutpoints after said final circuit netlist file met all timing constraints under said static timing analysis;

means for performing formal verification on said plurality of cutpoints;

means for determining whether or not said plurality of cutpoints pass said formal verification; ~~and~~

means for issuing a flag to alert a user, in response to a determination that said plurality of cutpoints do not pass said formal verification; and

means for sending said final circuit netlist file to manufacturing, in response to a determination that said plurality of cutpoints pass said formal verification.

14. (currently amended) The computer system of Claim 13, wherein said computer system further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, means for modifying said final netlist file ~~list~~ and returning to said performing static timing analysis with said modified final circuit netlist file.

15. (original) The computer system of Claim 13, wherein said computer system further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, means for modifying said snip file and returning to said converting said snip file with said modified snip file.

Please cancel Claim 16.

17. (original) The computer system of Claim 13, wherein said computer system for performing formal verification further includes means for performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

Please cancel Claim 18.